



100G QSFP28 LR4 Dual Rate Transceiver

Hot Pluggable, Duplex LC, LAN-WDM DFB, SMF 10KM, DDM

Part Number: FQ28-K7-L13-10DR



Overview:

FQ28-K7-L13-10DR is a 4-Channel LWDM 1300nm QSFP28 transceiver for 100GbE and OTU4 applications especially in Datacom, Data Center & Storage networks. The transmitter converts 4-Channel 28G electrical input data to four LWDM optical signals and multiplex that into one 112G signal. The receiver de-multiplex the 112G signal reversely and converts that to 4-Channel 28G electrical output data. The techniques bring a compact transceiver module for an aggregate bandwidth of 112Gbps up to SMF 10km optical links.

Applications:

- 100GBASE-LR4 Ethernet @103.1G
- OTN OTU4 @112.1G
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

Features:

- Compliant with IEEE 802.3ba 100GBASE-LR4
- Compliant with ITU G.959.1 OTU4 411-9D1F
- Compliant with SFF-8665 QSFP28 MSA
- Compliant with IEEE 802.3bm CAUI-4 Interface
- 4CH LWDM MUX / DEMUX design
- Data Rate up to 27.9525Gbps per Lane
- Built in quad TX CDR and RX CDR
- Hot Pluggable QSFP28 footprint
- O-Band LWDM DFB transmitter
- Duplex LC connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8636
- Single 3.3V power supply
- Link distance 10km over SM fiber
- Maximum Power consumption 4.0W
- RoHS compliant

Absolute Maximum Ratings:

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T _{ST}	-40	+85	°C
Storage Relative Humidity	RH	5	95	%
Supply Voltage	V _{CC3}	-0.5	+4.0	V



Recommended Operating Conditions:

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T _{OP}	0	-	+70	°C
Supply Voltage	V _{CC}	+3.13	+3.3	+3.47	V
Data Rate, per Lane	DR		25.78125	27.9525	Gb/s
Data Rate Accuracy (100GBASE-LR4)	ΔDR	-100		+100	ppm
Data Rate Accuracy (OTU4 411-9D1F)	ΔDR	-20		+20	ppm
Bit Error Rate	BER			5x10 ⁻⁵	
Supply Current	I _{CC}			1150	mA
Power Consumption	P			4.0	W
Transceiver Power-on Initialization Time				2000	ms
Control Input Voltage High	V _{IH}	2.0		V _{CC}	V
Control Input Voltage Low	V _{IL}	GND		0.8	V
Control Output Voltage High	V _{OH}	2.0		V _{CC}	V
Control Output Voltage Low	V _{OL}	GND		0.8	V

Transmitter Electro-optical Characteristics:

V_{CC}= 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
IEEE 802.3ba 100GBASE-LR4						
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Total Average Launch Power	TP _{AVG}			+10.5	dBm	
Average Launch Power, per Lane	P _{AVG}	-4.3		+4.5	dBm	
Optical Modulation Amplitude (OMA), per Lane	P _{OMA}	-1.3		+4.5	dBm	1
Difference in Launch Power between any two Lanes (OMA)	P _{TX-DIFF}			3.6	dB	
Transmitter Dispersion Penalty, per Lane	TDP			2.2	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), per Lane	OMA-TDP	-2.3			dB	1
ITU G.959.1 OTU4 411-9D1F						
Operating Data Rate, per Lane	DR		27.9525		Gb/s	
Total Average Launch Power	TP _{AVG}			+10.0	dBm	
Average Launch Power, per Lane	P _{AVG}	-0.6		+4.0	dBm	



IEEE 802.3ba 100GBASE-LR4 & ITU G.959.1 OTU4 4I1-9D1F						
Optical Wavelength, each Lane	λ_{L0}	1294.53	1295.56	1296.59	nm	
	λ_{L1}	1299.02	1300.05	1301.09	nm	
	λ_{L2}	1303.54	1304.58	1305.63	nm	
	λ_{L3}	1308.09	1309.14	1310.19	nm	
Spectral Width (-20dB)	$\Delta\lambda$			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Extinction Ratio	ER	4.0			dB	
Optical Eye Mask { X1, X2, X3, Y1, Y2, Y3 }		{ 0.25, 0.4, 0.45, 0.25, 0.28, 0.4 }				2
Average Launch Power OFF, per Lane	P _{OFF}			-30	dBm	
Relative Intensity Noise (OMA)	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	ORLT			20	dB	
Transmitter Reflectance	R _{TX}			-12	dB	
Input Differential Impedance	Z _{IN}	90	100	110	Ω	
Differential Data Input Voltage	V _{IN-PP}			900	mVpp	

Note1: Transmitter wavelength and launch power need to meet the OMA minus TDP specs to guarantee link performance.

Note2: Hit ratio 5×10^{-5} hits per sample.

Receiver Electro-optical Characteristics:

V_{CC}= 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
IEEE 802.3ba 100GBASE-LR4						
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Average Receive Power, per Lane	P _{RX-AVG}	-10.6		+4.5	dBm	
Receiver Power (OMA), per Lane	P _{RX-OMA}			+4.5	dBm	
Receiver Sensitivity (OMA), per Lane	SEN _{AVG}			-8.6	dBm	1
Stressed Receiver Sensitivity (OMA), per Lane	SEN _{SOMA}			-6.8	dBm	2
ITU G.959.1 OTU4 4I1-9D1F						
Operating Data Rate, per Lane	DR		27.9525		Gb/s	
Average Receive Power, per Lane	P _{RX-AVG}	-6.9		+4.0	dBm	3
Receiver Power (OMA), per Lane	P _{RX-OMA}	-8.6		+4.5	dBm	3
IEEE 802.3ba 100GBASE-LR4 & ITU G.959.1 OTU4 4I1-9D1F						



Damage Threshold, per Lane	D _{TH}	+5.5			dBm	4
Receiver Reflectance	R _{RX}			-26	dB	
LOS De-Assert	LOS _D			-11.6	dBm	
LOS Assert	LOS _A	-24			dBm	
LOS Hysteresis	LOS _{HY}	0.5		6	dB	
Receiver Electrical 3dB upper Cutoff Frequency, per Lane	F _{CUT}			31	GHz	
Output Differential Impedance	Z _{OUT}	90	100	110	Ω	
Differential Data Output Voltage	V _{OUT-PP}	400		800	mVpp	
Conditions of Stress Receiver Sensitivity Test (Note.4)						
Vertical Eye Closure Penalty, per Lane	VECP		1.8		dB	
Stressed Eye J2 Jitter, per Lane	J2		0.3		UI	5
Stressed Eye J9 Jitter, per Lane	J9		0.47		UI	5

Note1: Measured with conformance test signal at receiver input for BER= 5x10⁻⁵.

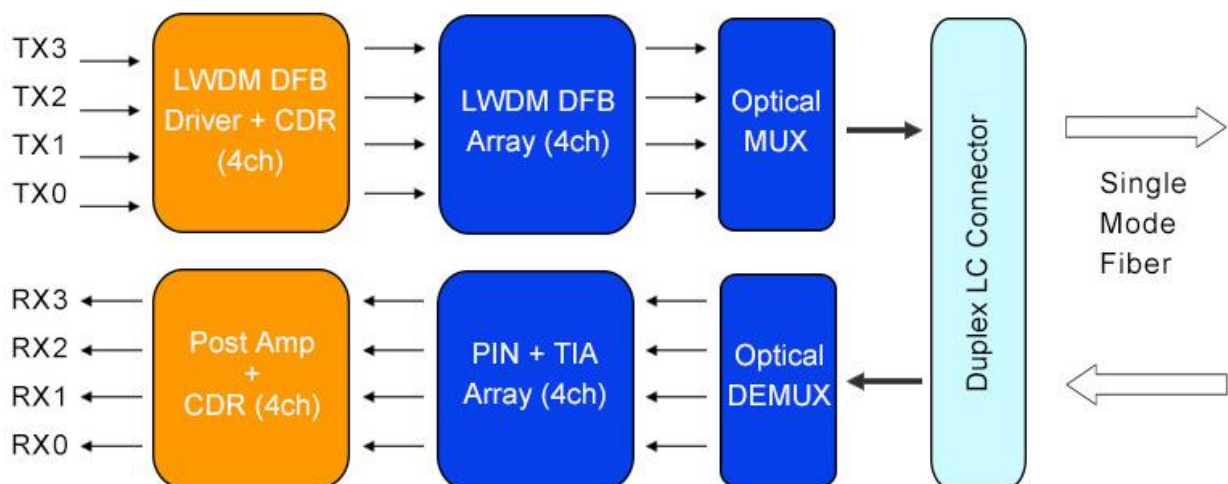
Note2: Measured with conformance test signal at receiver input for BER= 1x10⁻¹².

Note3: Measured with conformance test signal at receiver input for BER= 1x10⁻⁶.

Note4: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

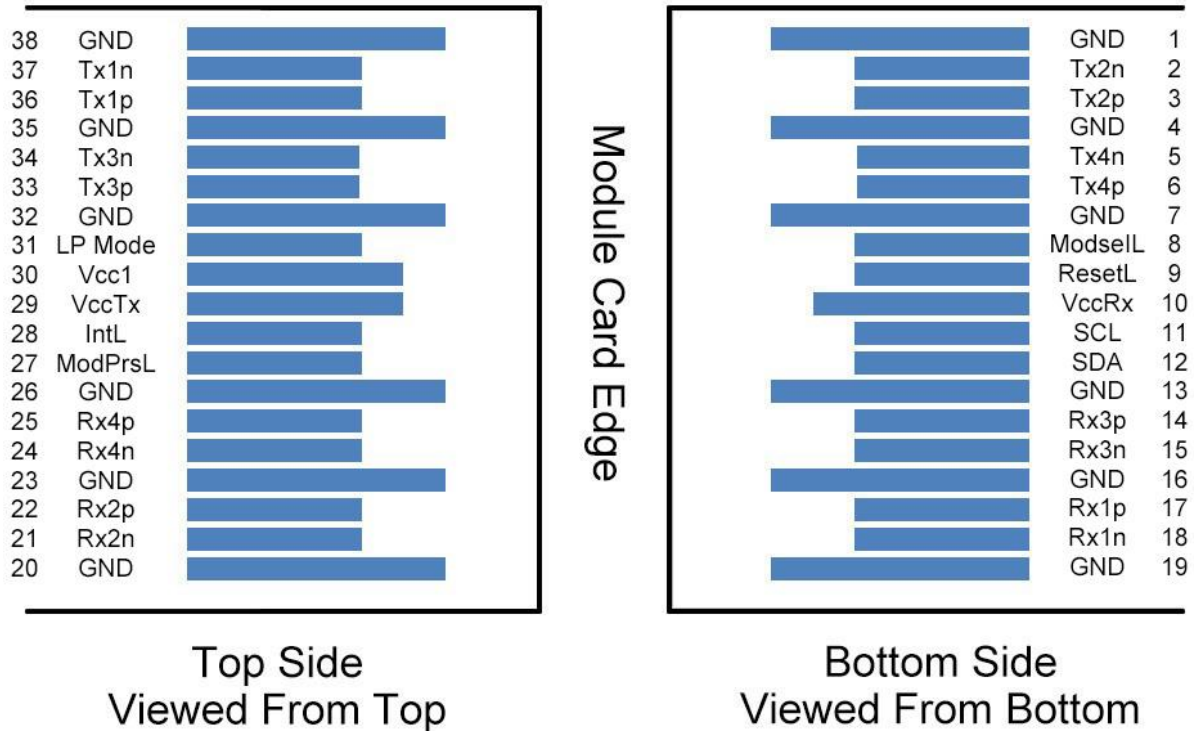
Note5: Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Transceiver Block Diagram:





Pin Assignment:



Pin Description:

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock



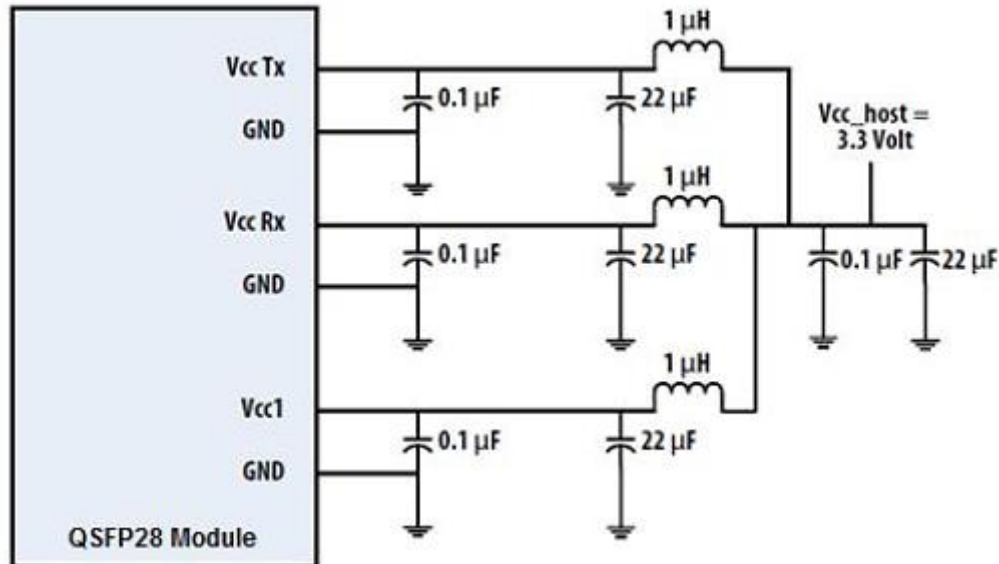
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMODE	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.



Recommended Power Supply Filter:



Digital Diagnostic Functions:

As defined by the QSFP28 MSA, Ficer's QSFP28 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

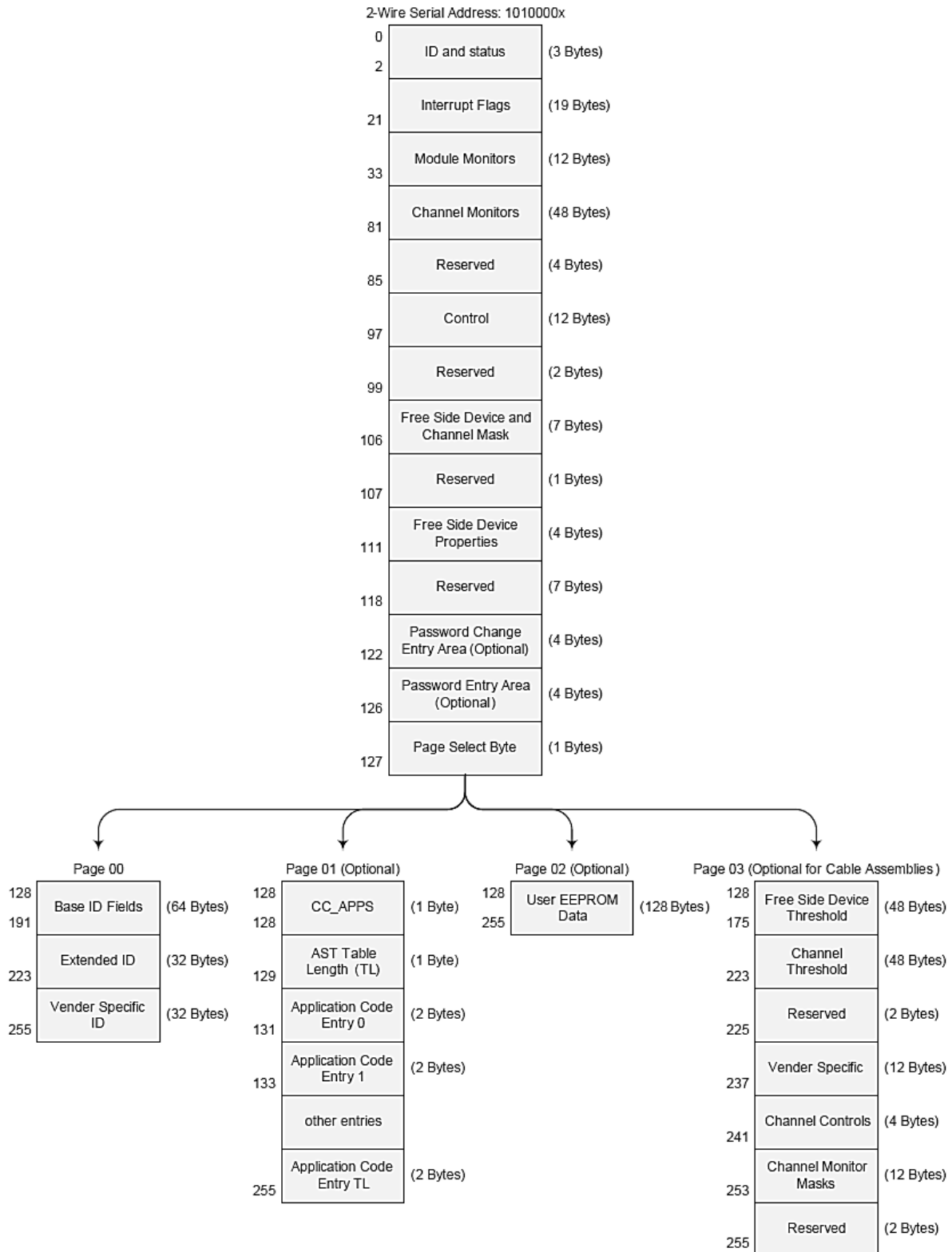
- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

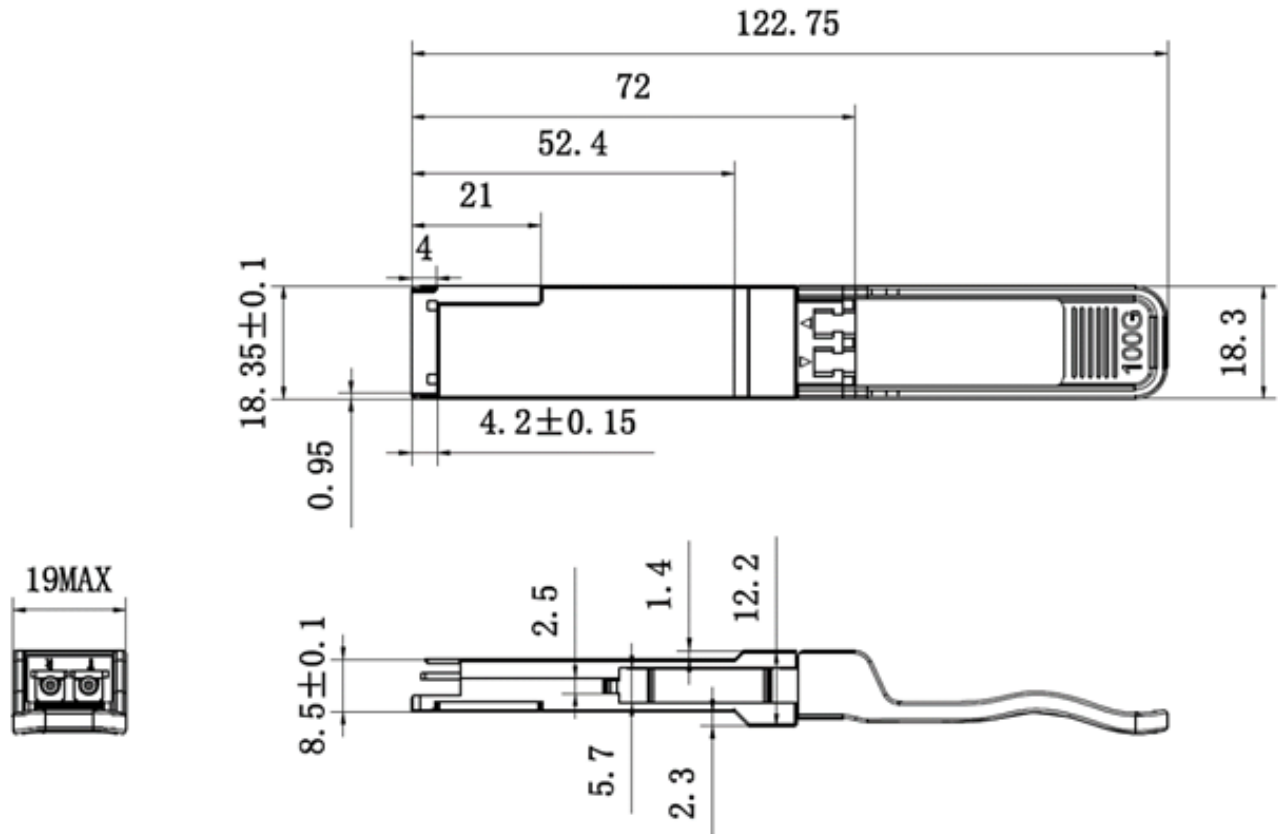
For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

Digital Diagnostic Memory Map





Mechanical Dimensions:



(All Dimensions are ± 0.20 mm Unless Otherwise Specified, Unit: mm)

Ordering Information:

Part No.	TX	RX	Link	DDM	Temp.
FQ28-K7-L13-10DR	1295.56 nm 1300.05 nm 1304.58 nm 1309.14 nm	1295.56 nm 1300.05 nm 1304.58 nm 1309.14 nm	10km	Yes	0~70°C

NOTE: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.