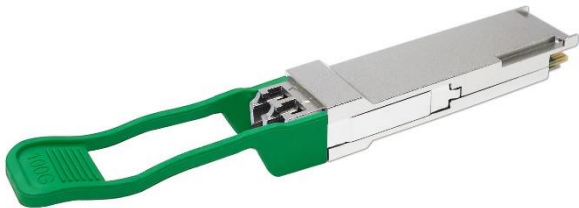




## 100G QSFP28 CWDM4 Transceiver

Hot Pluggable, Duplex LC, CWDM DFB, SMF 2KM, DDM

**Part Number:** FQ28-K7-C13-02D



### Overview:

FQ28-K7-C13-02D is a 4-Channel CWDM 1300nm QSFP28 transceiver for 100GbE applications especially in Datacom, Data Center & Storage networks. The transmitter converts 4-Channel 25G electrical input data to four CWDM optical signals and multiplex that into one 100G signal. The receiver de-multiplex the 100G signal reversely and converts that to 4-Channel 25G electrical output data. The techniques bring a compact transceiver module for an aggregate bandwidth of 100Gbps up to SMF 2km optical links.

### Applications:

- 100GBASE-CWDM4 application with FEC
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

### Features:

- Compliant with 100GBASE-CWDM4
- Compliant with SFF-8665 QSFP28 MSA
- Compliant with IEEE 802.3bm CAUI-4 Interface
- 4CH CWDM MUX / DEMUX design
- Data Rate 25.78125Gbps per Lane
- Built in quad TX CDR and RX CDR
- Hot Pluggable QSFP28 footprint
- CWDM DFB transmitter
- Duplex LC connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8636
- Single 3.3V power supply
- Link distance 2km over SM fiber with KR4 FEC
- Maximum Power consumption 3.5W
- RoHS compliant

### Absolute Maximum Ratings:

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T <sub>ST</sub>	-40	+85	°C
Storage Relative Humidity	RH	5	85	%
Supply Voltage	V <sub>CC</sub>	-0.5	+3.6	V



**Recommended Operating Conditions:**

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T <sub>OP</sub>	0	-	+70	°C
Supply Voltage	V <sub>CC</sub>	+3.13	+3.3	+3.47	V
Data Rate, per Lane	DR		25.78125		Gb/s
Data Rate Accuracy	ΔDR	-100		+100	ppm
Bit Error Rate	BER			5x10 <sup>-5</sup>	
Supply Current	I <sub>CC</sub>			1120	mA
Power Consumption	P			3.5	W
Transceiver Power-on Initialization Time				2000	ms
Control Input Voltage High	V <sub>IH</sub>	2.0		V <sub>CC</sub>	V
Control Input Voltage Low	V <sub>IL</sub>	GND		0.8	V
Control Output Voltage High	V <sub>OH</sub>	2.0		V <sub>CC</sub>	V
Control Output Voltage Low	V <sub>OL</sub>	GND		0.8	V

**Transmitter Electro-optical Characteristics:**

V<sub>CC</sub>= 3.13V to 3.47V, T<sub>OP</sub> = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Total Average Launch Power	TP <sub>AVG</sub>			+8.5	dBm	
Average Launch Power, per Lane	P <sub>AVG</sub>	-6.5		+2.5	dBm	
Optical Modulation Amplitude (OMA), per Lane	P <sub>OMA</sub>	-4.0		+2.5	dBm	1
Difference in Launch Power between any two Lanes (OMA)	P <sub>TX-DIFF</sub>			5.0	dB	
Transmitter Dispersion Penalty, per Lane	TDP			3.0	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty, per Lane	OMA-TDP	-5.0			dB	1
Optical Wavelength, each Lane	λ <sub>L0</sub>	1264.5	1271	1277.5	nm	
	λ <sub>L1</sub>	1284.5	1291	1297.5	nm	
	λ <sub>L2</sub>	1304.5	1311	1317.5	nm	
	λ <sub>L3</sub>	1324.5	1331	1337.5	nm	
Spectral Width (-20dB)	Δλ			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Optical Extinction Ratio	ER	3.5			dB	



Optical Eye Mask { X1, X2, X3, Y1, Y2, Y3 }		{ 0.31, 0.4, 0.45, 0.34, 0.38, 0.4 }				2
Average Launch Power OFF, per Lane	P <sub>OFF</sub>			-30	dBm	
Optical Return Loss Tolerance	ORLT			20	dB	
Transmitter Reflectance	R <sub>TX</sub>			-12	dB	
Input Differential Impedance	Z <sub>IN</sub>	90	100	110	Ω	
Differential Data Input Voltage	V <sub>IN-PP</sub>	900		1600	mVpp	

**Note1:** Transmitter wavelength and launch power need to meet the OMA minus TDP specs to guarantee link performance.

**Note2:** Hit ratio  $5 \times 10^{-5}$  hits per sample.

### Receiver Electro-optical Characteristics:

V<sub>CC</sub>= 3.13V to 3.47V, T<sub>OP</sub> = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Lane	DR		25.78125		Gb/s	
Damage Threshold, per Lane	D <sub>TH</sub>	+3.5			dBm	1
Average Receive Power, per Lane	P <sub>RX-AVG</sub>	-11.5		+2.5	dBm	
Receive Sensitivity (OMA), per Lane	SEN <sub>OMA</sub>			-10.0	dBm	2
Stressed Receiver Sensitivity (OMA), per Lane	SEN <sub>SOMA</sub>			-7.3	dBm	3
Optical Wavelength, each Lane	λ <sub>L0</sub>	1264.5		1277.5	nm	
	λ <sub>L1</sub>	1284.5		1297.5	nm	
	λ <sub>L2</sub>	1304.5		1317.5	nm	
	λ <sub>L3</sub>	1324.5		1337.5	nm	
Receiver Reflectance	R <sub>RX</sub>			-26	dB	
LOS De-Assert	LOS <sub>D</sub>			-13.6	dBm	
LOS Assert	LOS <sub>A</sub>	-24			dBm	
LOS Hysteresis	LOS <sub>HY</sub>	0.5		6	dB	
Output Differential Impedance	Z <sub>OUT</sub>	90	100	110	Ω	
Differential Data Output Voltage	V <sub>OUT-PP</sub>	400		800	mVpp	
Conditions of Stress Receiver Sensitivity Test (Note.4)						
Vertical Eye Closure Penalty, per Lane	VECP	1.9			dB	
Stressed Eye J2 Jitter, per Lane	J2	0.33			UI	4
Stressed Eye J4 Jitter, per Lane	J4	0.48			UI	4
SRS Eye Mask { X1, X2, X3, Y1, Y2, Y3 }		{ 0.39, 0.5, 0.5, 0.39, 0.39, 0.4 }				

**Note1:** The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical



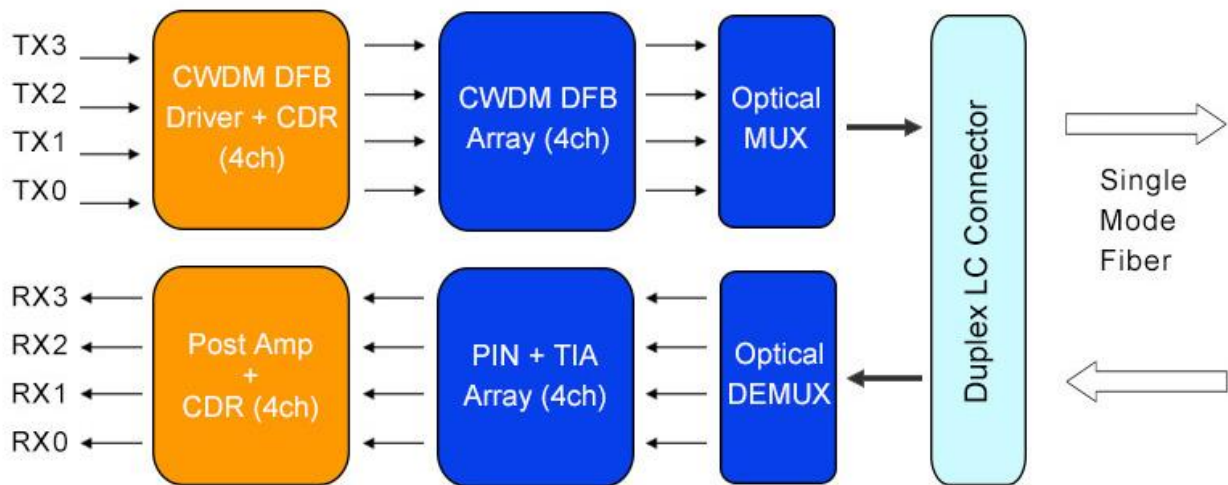
input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

**Note2:** Measured with conformance test signal at receiver input for BER=  $5 \times 10^{-5}$ .

**Note3:** Measured with conformance test signal at receiver input for BER=  $1 \times 10^{-12}$ .

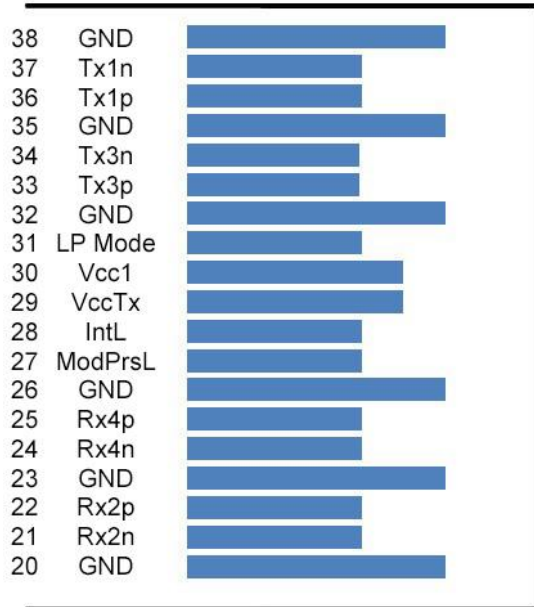
**Note4:** Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

## Transceiver Block Diagram:



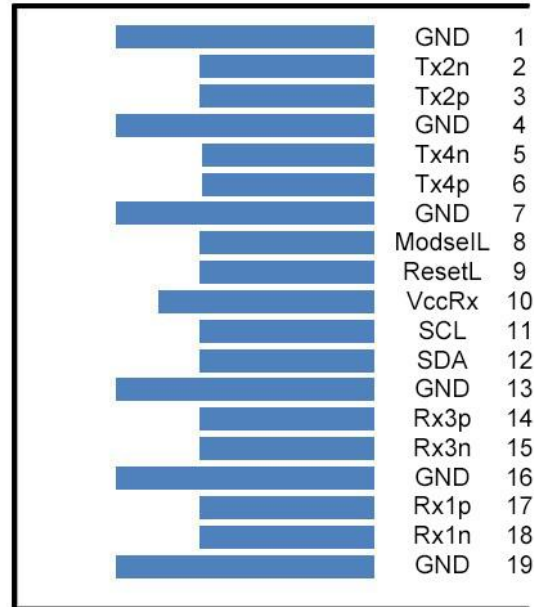


## Pin Assignment:



Top Side  
Viewed From Top

Module Card Edge



Bottom Side  
Viewed From Bottom

## Pin Description:

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock



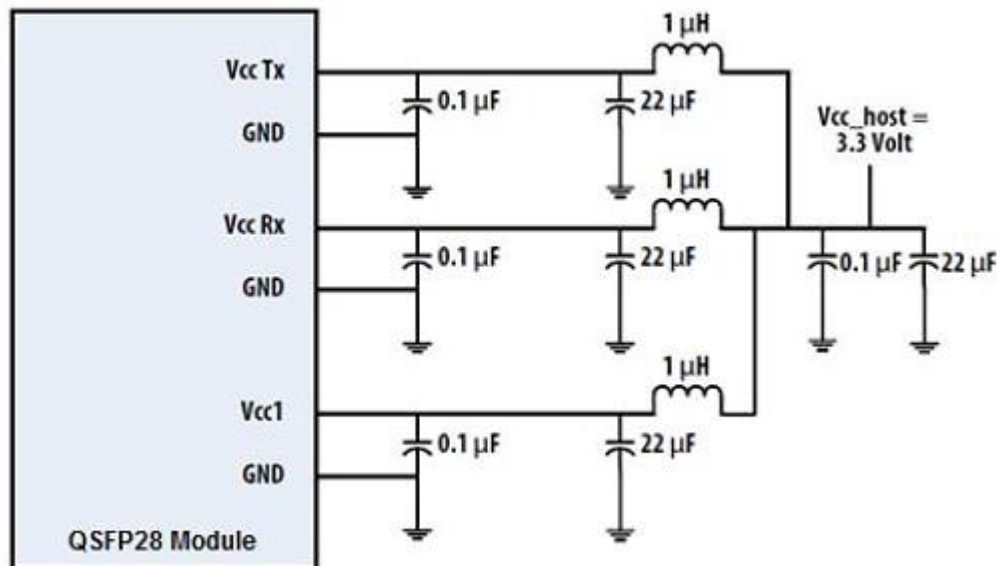
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMODE	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

**Note1:** GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

**Note2:** VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.



## Recommended Power Supply Filter:



## Digital Diagnostic Functions:

As defined by the QSFP28 MSA, Ficer's QSFP28 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

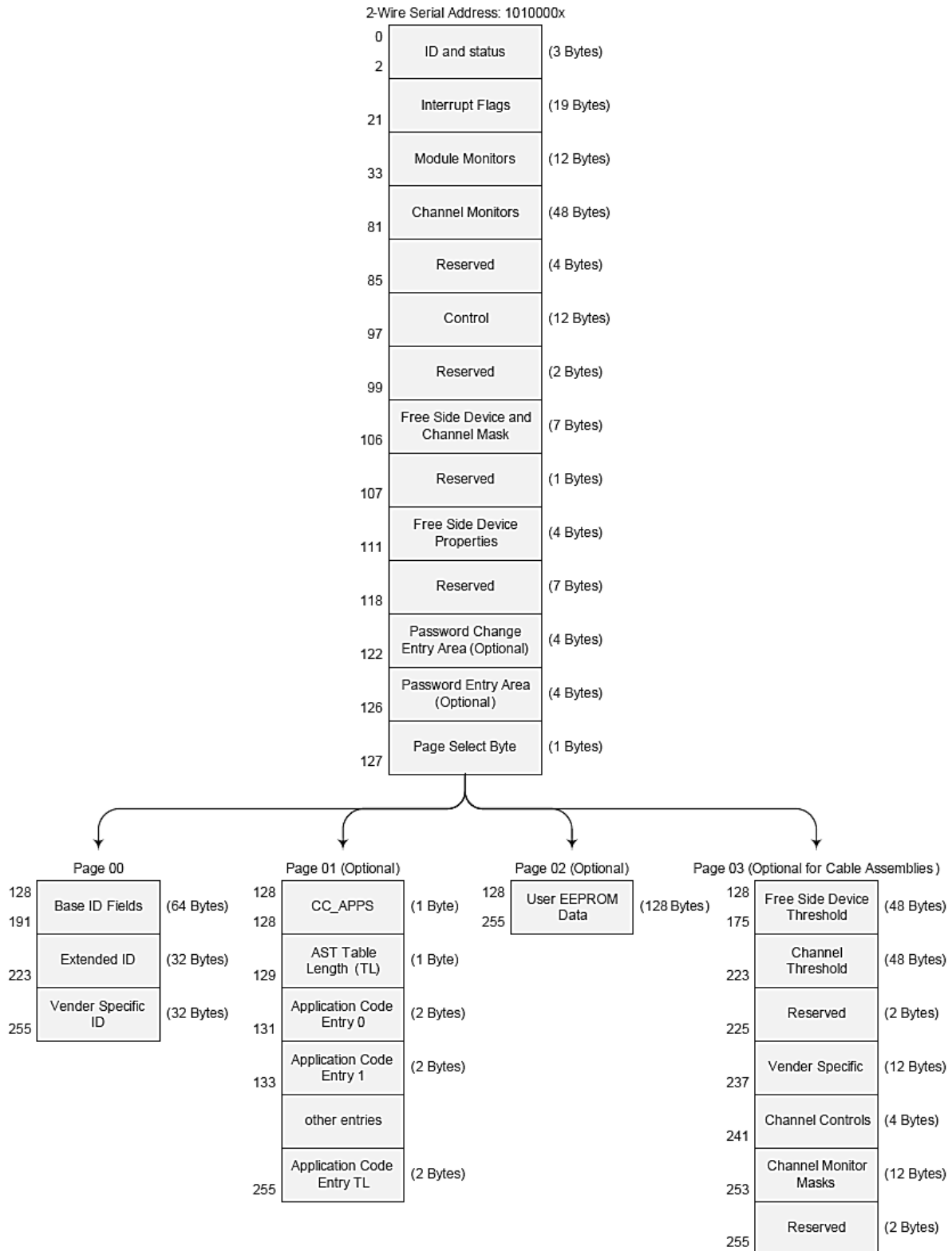
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8-bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

## QSFP28 Digital Diagnostic Memory Map

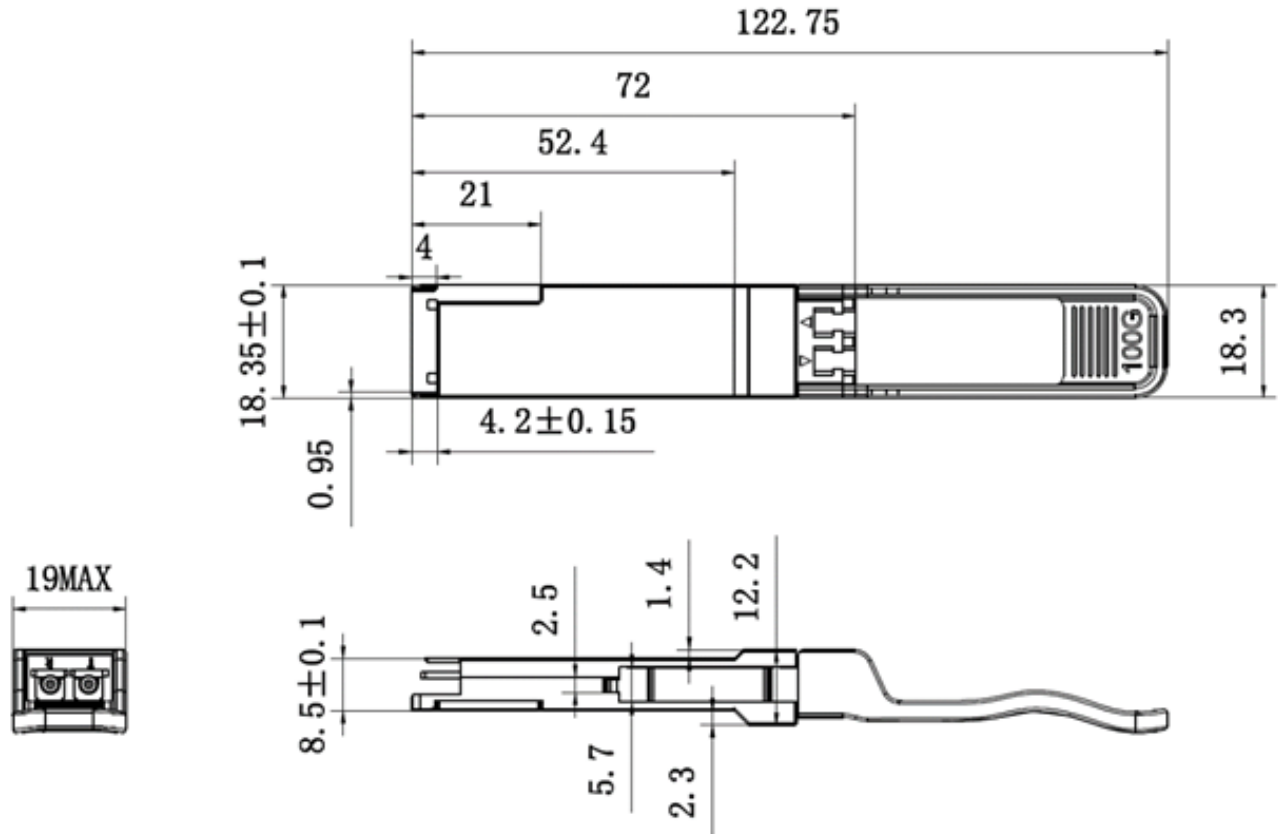








## Mechanical Dimensions:



(All Dimensions are  $\pm 0.20$ mm Unless Otherwise Specified, Unit: mm)

## Ordering Information:

Part No.	TX	RX	Link	DDM	Temp.
FQ28-K7-C13-02D	1271nm 1291nm 1311nm 1331nm	1271nm 1291nm 1311nm 1331nm	2km	Yes	0~70°C

**NOTE:** Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.